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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,219	07/31/2003	Thomas McDonald	CNTR.2144	2086

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EXAMINER	
MOLL, JESSE R	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	10/632,219	MCDONALD, THOMAS	
	Examiner	Art Unit	
	Jesse R. Moll	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Fritz Fleming
FRITZ FLEMING
Supervisory PRIMARY EXAMINER
GROUP 2100
4/2/2006
AU 2181

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *31 July 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-23 have been examined.

Acknowledgment of papers filed: oath, specification, drawings, and IDS, on July 31, 2003. The papers filed have been placed on record.

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 22 and 23 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 24 recites the limitation "a computer data signal embodied in a transmission medium". A computer data signal embodied in a transmission medium does not fall under any of the statutory classes. First, a claimed signal is clearly not a "process" under Sec. 101 because it is not a series of steps. The other three Sec. 101 classes of machine, compositions of matter and manufactures "relate to structural entities and can be grouped as `product' claims in order to contrast them with process claims." 1 D. Chisum, Patents Sec. 1.02 (1994). The three product classes have traditionally required physical structure or material.

Examiner suggests (and assumes for the purpose of examination) that the limitation "A computer data signal embodied in a transmission medium" read "A

computer program embodied on a computer readable medium". The term computer usable (e.g., readable) medium as defined in Applicant's specification (page 47, lines 8-11) does not include non-tangible signals.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 9-17 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9 recites the limitation "said instruction cache". There is insufficient antecedent basis for this limitation in the claim.

Claims 10-17 are rejected as being dependent on indefinite parent claims.

Further, claim 17 recites the limitation "substantially conforms to". This limitation is vague and it is unclear what is meant by "substantially" or how close to conforming to the x86 specification would fall under the scope of the claim.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-13 and 16-23 are rejected under 35 U.S.C. 102(b) as being anticipated by White (U.S. Patent No. 5,734,881).

6. Regarding claim 1, White discloses a deadlock avoidance apparatus in a microprocessor having a speculative branch target address cache (BTAC) (BTC 252; see fig. 2a), the apparatus comprising: a first signal (see col. 18, lines 21-31), for indicating a miss of a fetch address (if it is not a short COF) in an instruction cache (prefetch buffer 242; see fig. 2a; see cols. 11-12, section 2.1),

Note that the prefetch buffer is considered a cache because the definition of cache according to The American Heritage® Dictionary of the English Language, Fourth Edition is "A fast storage buffer in the central processing unit of a computer." Therefore, this prefetch buffer can be considered a cache.

Wherein said fetch address is a speculative branch instruction target address (see col. 22, lines 20-23) provided by the BTAC (see col. 12, lines 1-10); a second signal (if the situation is detected, there must be a signal), for indicating said branch instruction wraps across two cache lines (see col. 22, lines 64-66); and a third signal, for

indicating the BTAC predicted said branch instruction does not wrap across said two cache lines (see col. 22, lines 55-67),

Note that the second line may not be fetched. Therefore, it can be said that it is predicted (either statically or dynamically) that the instruction will not wrap across two cache lines. Further note that in the case of a static prediction, the signal would be the signal indicating a hit in the BTC. In the case of dynamic prediction, a signal would have to be used to indicate whether the instruction is predicted to wrap across two cache lines.

Whereby a second of said two cache lines is not fetched because the BTAC predicted said branch instruction does not wrap across said two cache lines (see col. 22, lines 55-67); and control logic, coupled to receive said first, second, and third signals, for invalidating said target address in the BTAC (see col. 23, lines 1-5),

Note that the address marked by the TARG flag is the target address (the same address that is in the BTC). That address is invalidated in the new CURR buffer. Therefore, said target address (which is in the BTAC) is invalidated.

In response to a true indication on said first, second, and third signals.

Note that the address is invalidated when, a branch instructions wraps across 2 lines, a target address misses in the cache (normal COF instead of short COF), and the instruction is predicted not to wrap across two lines.

7. Regarding claim 2, White discloses the apparatus of claim 1, wherein said control logic is further configured to cause the microprocessor to branch to said branch

instruction after said invalidating said target address in the BTAC (see col. 23 lines 2-3 regarding fetching the rest of the branch instruction.).

Note that fetching the instruction is considered branching to it. Branch instructions set the fetch pointer to a certain location.

8. Regarding claim 3, White discloses the apparatus of claim 1, wherein an instruction formatter determines said branch instruction wraps across said two cache lines by decoding a first of said two cache lines (see col. 22, lines 64-66).

9. Regarding claim 4, White discloses the apparatus of claim 3, wherein said instruction cache provides said first of said two cache lines (see col. 22, lines 55-66).

10. Regarding claim 5, White discloses the apparatus of claim 1, wherein said branch instruction target address is speculative because said target address is only, a prediction and is not guaranteed to be a correct target address of said branch instruction (see col. 26, lines 60-65).

11. Regarding claim 6, White discloses the apparatus of claim 1, wherein said branch instruction target address is speculative because said target address may be a target address of a different branch instruction (see col. 17, lines 44-51).

12. Regarding claim 7, White discloses the apparatus of claim 1, wherein said branch instruction target address is speculative because said branch instruction may not be present in said two cache lines (see col. 25, lines 6-14).

13. Regarding claim 8, White discloses the apparatus of claim 1, wherein said second of said two cache lines is not fetched comprises said second of said two cache lines is not fetched from a memory coupled to the microprocessor (Inherently, if it is not fetched, it not fetched from a memory coupled to the microprocessor.).

14. Regarding claim 9, White discloses a pipelined microprocessor for avoiding a deadlock condition, comprising: a branch target address cache (BTAC) (BTC 252; see fig. 2a), for providing a speculative target address (see col. 18, lines 50-57) of a branch instruction (COF) in response to an instruction cache fetch address (see col. 18, lines 42-45); and control logic, coupled to said BTAC, for invalidating said speculative target address in said BTAC (see col. 23, lines 1-5; see above regarding claim 1) in response to detecting a condition in which: said speculative target address misses in an instruction cache (see col. 18, lines 21-31; see above regarding claim 1) after said instruction cache provides a first cache line in response to said fetch address (see col. 22, lines 64-66),

Note that if the instruction starts to decode, the first line must have been provided to the decoder.

Wherein said first cache line contains only a first portion of said branch instruction (see fig. 5c, col. 22, lines 28-33); and said BTAC incorrectly predicts that said branch instruction is wholly contained within said first cache line (see col. 22, lines 64-66; see above regarding claim 1), thereby causing a second cache line containing a second portion of said branch instruction not to be fetched from said instruction cache (see col. 22, lines 55-67).

15. Claim 10 recites equivalent limitations as claim 2 and is therefore rejected under the same grounds.

16. Regarding claim 11, White discloses the microprocessor of claim 9, further comprising: an instruction fetcher, coupled to said control logic, for fetching missing cache lines into said instruction cache (see col. 24, lines 18-23) from a memory coupled to the microprocessor, wherein said instruction fetcher is configured not to fetch missing cache lines from speculative target addresses provided by said BTAC (see col. 24, lines 60-64).

Note that the instruction fetcher is configured not to fetch missing cache lines if they are not available in the L1 cache. The claim does not state that no speculative instructions can be fetched.

17. Regarding claim 12, White discloses the microprocessor of claim 9, further comprising: an instruction formatter, coupled to said control logic (ID 211, see figs. 2a

and 3), for decoding said first cache line (see col. 22, lines 64-66) and generating a signal to said control logic indicating said branch instruction is not wholly contained within said first cache line (if this condition is known, there must be a signal indicating it).

18. Regarding claim 13, White discloses the microprocessor of claim 12, further comprising: an instruction buffer (Latch 326; see fig. 4a), coupled to said instruction cache (see fig. 4a), for receiving said first cache line from said instruction cache (see col. 24, lines 60-64)

Note that the entire cache line is not received at the same time, but the entire line is still received.

And storing said first cache line while said instruction formatter decodes said first cache line (see col. 12, lines 58-67).

Note that the entire cache line is not stored at the same time, but the entire line is still stored.

19. Regarding claim 16, White discloses the microprocessor of claim 9, wherein an instruction set of the microprocessor comprises instructions of variable length (see col. 12, lines 1-3).

Regarding claim 17, White discloses the microprocessor of claim 9, wherein said instruction set conforms to an x86 architecture instruction set (see col. 7, lines 3-4).

20. Regarding claim 18, White discloses a method for avoiding a deadlock condition in a microprocessor having an instruction cache (prefetch buffer 242; see fig. 2a; see cols. 11-12, section 2.1; see above regarding claim 1) and a speculative branch target address cache (BTAC) (BTC 252; see fig. 2a), the method comprising: generating a speculative target address of a branch instruction (see col. 22, lines 20-23) partially contained in a first cache line (see fig. 5c, col. 22, lines 28-33) provided by the instruction cache (see col. 22, lines 64-66)

Note that if the instruction starts to decode, the first line must have been provided to the decoder.

In response to a first fetch address (address of first line), in response to applying the first fetch address to the BTAC; providing said target address (address of COF target) as a second fetch address to the instruction cache (see col. 21, lines 3-6) without fetching a next cache line sequential to the first cache line (see col. 22, lines 55-63), in response to the BTAC predicting the branch instruction is wholly contained in the first cache line (see above regarding claim 1); determining the BTAC incorrectly predicted the branch instruction is wholly contained in the first cache line (see col. 22, lines 55-67; see above regarding claim); detecting a miss of the target address in the instruction cache (if it is not a short COF; see above regarding claim 1); and invalidating the target address in the BTAC, in response to said determining and said detecting (see col. 23, lines 1-5; see above regarding claim 1).

21. Claim 19 recites equivalent limitations as claim 2 and is therefore rejected under the same grounds.

22. Regarding claim 20, White discloses the method of claim 19, wherein said branching the microprocessor to an address of the branch instruction comprises providing the first fetch address to the instruction cache as a next fetch address (see col. 23, lines 1-5).

23. Regarding claim 21, White discloses the method of claim 19, wherein said branching the microprocessor to an address of the branch instruction comprises assigning the address of the branch instruction to an instruction pointer register of the microprocessor (see col. 14, lines 53-58).

Note that the instruction pointer points to what is being decoded. Therefore, when a COF wraps across two cache lines, the second half of the instruction must be decoded and therefore the instruction pointer will point to it.

24. Claim 22 recites equivalent limitations as claim 1 and is therefore rejected under the same grounds.

25. Claim 23 recites equivalent limitations as claim 1 and is therefore rejected under the same grounds.

Allowable Subject Matter

26. Claims 14 and 15 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Claim 14 recites the limitation "wherein said execution logic does not detect said BTAC incorrectly predicts that said branch instruction is wholly contained within said first cache line because said instruction formatter stalls waiting for said second cache line to be fetched." The prior art does not teach or fairly suggest not detecting said BTAC incorrectly predicts that said branch instruction is wholly contained within said first cache line because said instruction formatter stalls waiting for a second cache line to be fetched.

Claim 15 is dependent on claim 14, and is therefore is allowable subject matter for the same reasons.

Conclusion

27. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the

claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse R. Moll whose telephone number is (571)272-2703. The examiner can normally be reached on M-F 8:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on 571-272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JM 3/27/05

Supervisory

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9/2/2006